ABSTRACT

A thin film transistor array substrate, and manufacturing methods thereof, having a dual data link structure comprised of a first data link made from a gate metal layer and of a second data link made from a transparent conductive layer. A gate pad made from the gate metal layer electrically connects directly with the first data link, and to the second data link via a data pad protection electrode that passes through contact holes. The data pad protection electrode makes surface connections to the data pad. A data line is electrically connected via a contact electrode to the first data link. The data line and the data pad are formed from different metal layers. The data pad is protected by a gate insulating layer. The contact electrode is extended from the second data link.